CURRENT STATUS OF THE CLAIMS

In the Claims

The following is a marked-up version of the claims with the language that is underlined ("___") being added and the language that contains strikethrough ("—") being deleted:

1. (Amended) A chip-level electronic package, comprising:

at least one waveguide having a waveguide core, an air-gap cladding around a portion of the waveguide core, and an overcoat layer engaging a portion of the air-gap cladding.

2. (Canceled)

3. (Amended) The chip-level electronic package of claim ~~2~~ 1, further comprising:

a lead; and

at least one air-gap layer disposed substantially under a portion of the lead and wherein the at least one waveguide is adjacent the air-gap layer.

4-5. (Canceled)

6. (Amended) The chip-level electronic package of claim ~~2~~ 1, further comprising:

a coupling element adjacent to the waveguide core and engaging the air-gap cladding.

7. The chip-level electronic package of claim 1, wherein the waveguide core includes at least one coupling element.

8. The chip-level electronic package of claim 7, wherein the at least one coupling element is a volume grating coupling element.

9. (Amended) The chip-level electronic package of claim 7, ~~further comprising:~~

wherein the ~~an~~ air-gap cladding is disposed around a portion of one of the ~~waveguide cores~~ at least one coupling element.

10-14. (Canceled)

15. The chip-level electronic package of claim 1, wherein the waveguide core is adjacent to a lower waveguide cladding.

16-28 (Canceled)

29. (Amended) A method of operating a chip-level electronic package comprising:

coupling an optical signal to a waveguide in the wafer-level electronic package; and

communicating the optical signal through the waveguide, the waveguide having a waveguide core, an air-gap cladding around a portion of the waveguide core, and an overcoat layer engaging a portion of the air-gap cladding.

30. (Canceled)

31. (Newly Added) The chip-level electronic package of claim 1, wherein the overcoat layer is selected from silicon dioxide, silicon nitride, polyimides, polynorbornenes, epoxides, polyarylenes ethers, and parylenes.

32. (Newly Added) The chip-level electronic package of claim 1, wherein the overcoat layer is selected from polyimides, polynorbornenes, epoxides, polyarylenes ethers, and parylenes.

33. (Newly Added) The chip-level electronic package of claim 1, wherein the overcoat layer is selected from polyimides and polynorbornenes.

34. (Newly Added) A chip-level electronic package, comprising:

at least one waveguide having a waveguide core, a sacrificial layer around a portion of the waveguide cores, and an overcoat layer engaging a portion of the sacrificial layer.

35. (Newly Added) The chip-level electronic package of claim 34, wherein the overcoat layer is selected from silicon dioxide, silicon nitride, polyimides, polynorbornenes, epoxides, polyarylenes ethers, and parylenes.

36. (Newly Added) The chip-level electronic package of claim 34, wherein the sacrificial layer is selected from polyimides, polynorbornenes, epoxides, polyarylenes ethers, and parylenes.

37. (Newly Added) The chip-level electronic package of claim 34, wherein the sacrificial layer is selected from polypropylene carbonate, polyethylene carbonate, polynorborene carbonate.

38. (Newly Added) The chip-level electronic package of claim 34, further comprising:

a coupling element adjacent to the waveguide core and engaging the sacrificial layer.

39. (Newly Added) The chip-level electronic package of claim 34, wherein the waveguide core includes at least one coupling element.

40. (Newly Added) The chip-level electronic package of claim 39, wherein the at least one coupling element is a volume grating coupling element.

41. (Newly Added) The chip-level electronic package of claim 34, wherein the sacrificial layer is disposed around a portion of one of the at least one coupling element.